Controlled Layer Removal in Plasma Pseudo-Atomic Layer Etching

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Abstract: The goal of Atomic Layer Etching (ALE) is removal of single or fraction of a layer of material in a cyclic fashion. Although precise, ALE is also slow. In this work, we investigated pseudo-ALE, in which a controlled amount of material is removed during pulsed processing, with the intent of speeding the etch rate. Results are discussed for psuedo-ALE of silicon in Ar/Cl_2-pulsed and CW inductively coupled plasmas with pulsed biases.

1. Introduction

Plasma based Atomic Layer Etching (ALE) is used in fabrication of microelectronic devices where high precision is required. ALE of silicon consists of cyclic repetition of two self-limiting steps: passivation, where the material (e.g., silicon) is ideally passivated by the ion-free flux of radicals (Cl passivating Si to form $SiCl_x$), and etching, where the passivated layer is selectively removed by an ion-rich flux with energy tuned to remove only the passivated layer [1]. Although precise, ALE is also slow due to the need to evacuate the chamber between steps. Pseudo-ALE (P-ALE) is a process whereby a controlled amount of material is removed during pulsed processing. Although not as precise as conventional ALE, PALE has the advantage of higher rate and throughput. We discuss results from a computational investigation of P-ALE of silicon.

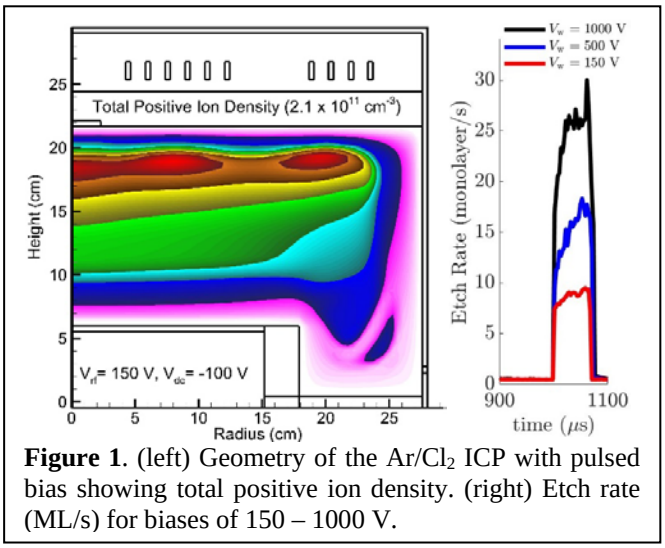

Figure 1. (left) Geometry of the Ar/Cl_2 ICP with pulsed bias showing total positive ion density. (right) Etch rate (ML/s) for biases of 150 – 1000 V.

2. Description of the Models

This investigation used the Hybrid Plasma Equipment Model (HPEM) to simulate the ICP reactor with base-case conditions 1000 W source power at 30 mTorr in an Ar/Cl_2 = 70/30 mixture. The 30 cm wafer is biased with pulsed, 10 MHz RF voltage. Si etch rates were evaluated using the Surface Kinetics Module in the HPEM with the mechanism from Huard et al. [2] renormalized using experiments by Chang et al. [3]. Feature profile evolution was evaluated with the Monte Carlo Feature Profile Model [2].

3. P-ALE of Si in Ar/Cl_2 ICPs

The reactor geometry and total positive ion density for the base case are shown in Fig. 1. The substrate voltage for a constant 150 V (DC bias -100 V) bias produces an etch rate of 6 monolayers per second (ML/s). Pulsed biases of 150 V, 500 V, and 1000 V at a pulse repetition frequency of 5 kHz were considered. The etch rates as a function of pulsed bias voltage for a duty cycle of 33% are shown in Fig. 1. For these conditions with CW etching the process nominally operates in the ion starved regime. That is, there is sufficient Cl flux to the surface to passivate the Si. Removal of the passivation is then limited by ion bombardment. Ion activation scales with the square root of ion energy. The increase in etch rate (7-8 ML/s to 26 ML/s) is largely due to the increase in incident ion energy with increasing bias. However, for large substrate biases, there is also an increase in ion flux. During the bias-off portion of the cycle, the etch rate is non-zero due to the moderate plasma potential that accelerate ions into the substrate. Although undesirable from a precision perspective, the absolute etch rate is small and so the total removal of material is controlled by the pulsed bias.

For sufficiently large bias voltage with long enough pulses, the system transitions into a neutral starved regime. In this regime the surface is not re-passivated by the constant Cl flux, and the etch rate decreases. This would be the P-ALE regime. Combinations of voltage amplitude, pulse length and Cl fluxes produce ALE-like conditions that rapidly remove a given amount of material.

4. Conclusion

In this study, we computationally investigated the P-ALE of silicon in ICPs using Ar/Cl_2 mixtures. Combinations of bias voltage, pulse length and Cl fluxes enable rapid removal of controllable amounts of material.

Acknowledgement

This work was supported by Samsung Electronics.

References

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